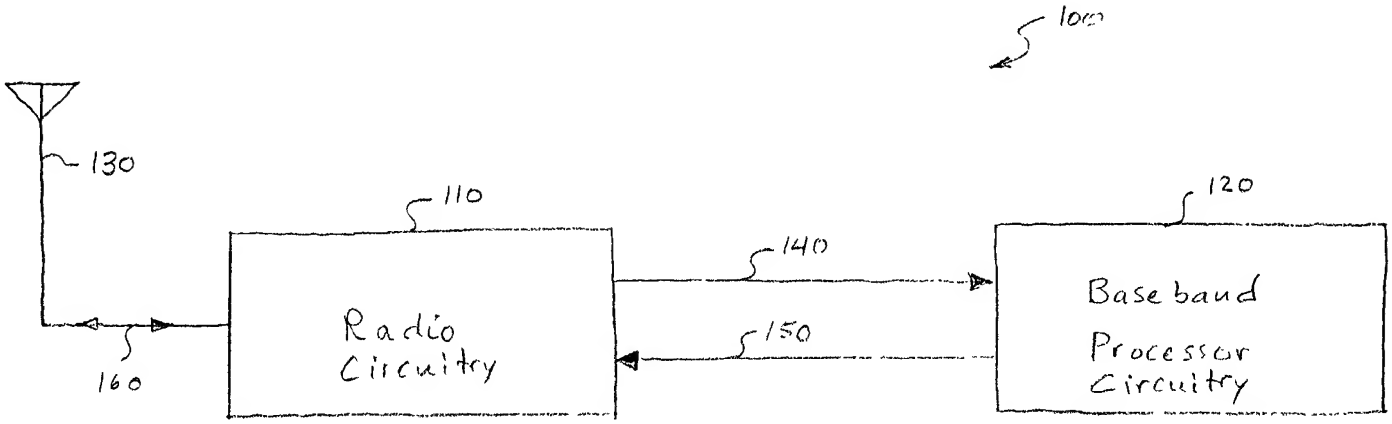


FIG. 1

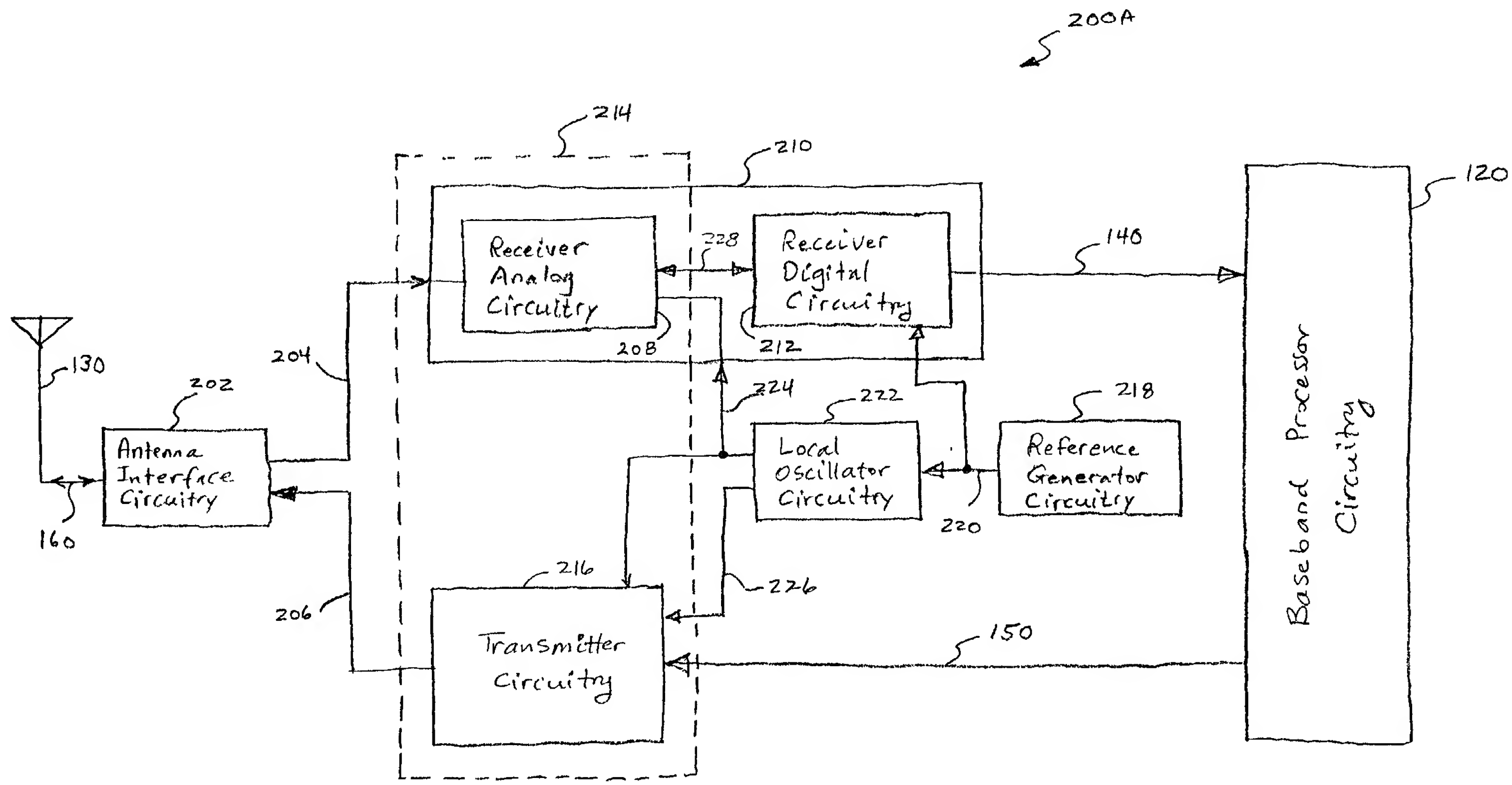

200A
214
210
120
Receiver Analog Circuitry
228
Receiver Digital Circuitry
140
130
202
204
208
212
224
222
218
Antenna Interface Circuitry
Local Oscillator Circuitry
Reference Generator Circuitry
Baseband Processor Circuitry
160
220
216
226
206
Transmitter Circuitry
150

FIG. 2A

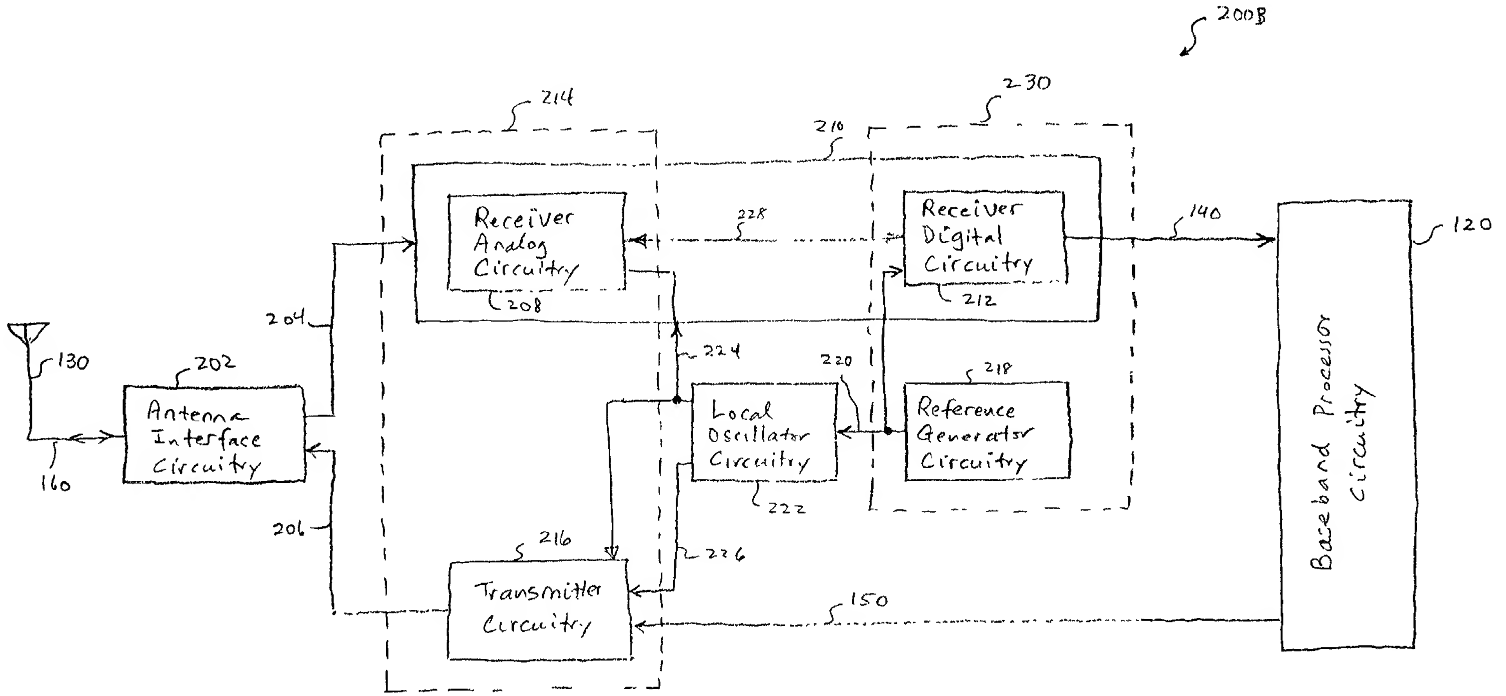

200B
214
210
230
Receiver Analog Circuitry
208
228
Receiver Digital Circuitry
212
140
120
Baseband Processor Circuitry
130
202
Antenna Interface Circuitry
160
204
206
224
220
218
Local Oscillator Circuitry
222
Reference Generator Circuitry
216
Transmitter Circuitry
226
150

FIG. 2B

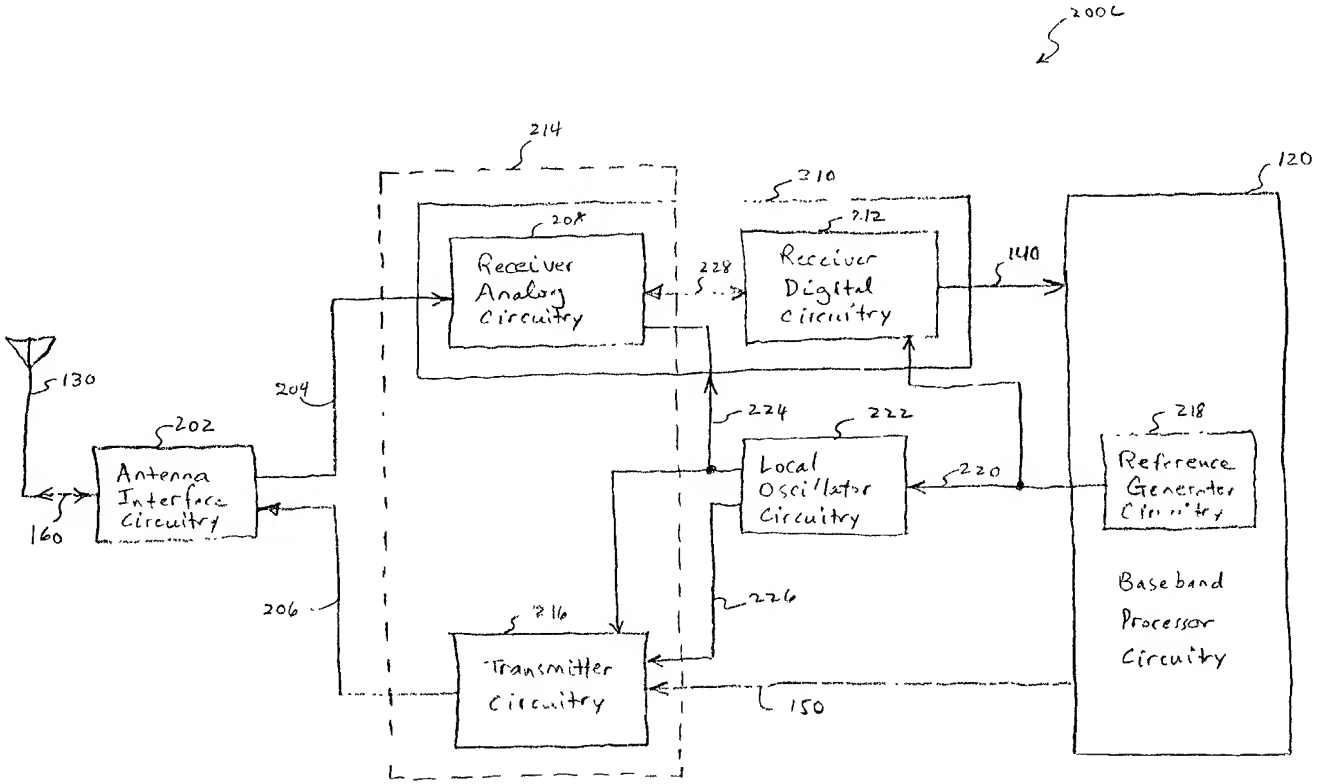

200C
214
120
210
208
212
Receiver Analog Circuitry
228
Receiver Digital circuitry
140
130
204
202
224
222
218
Antenna Interface Circuitry
Local Oscillator Circuitry
220
Reference Generator Circuitry
160
206
226
216
Transmitter Circuitry
Baseband Processor Circuitry
150

FIG. 2C

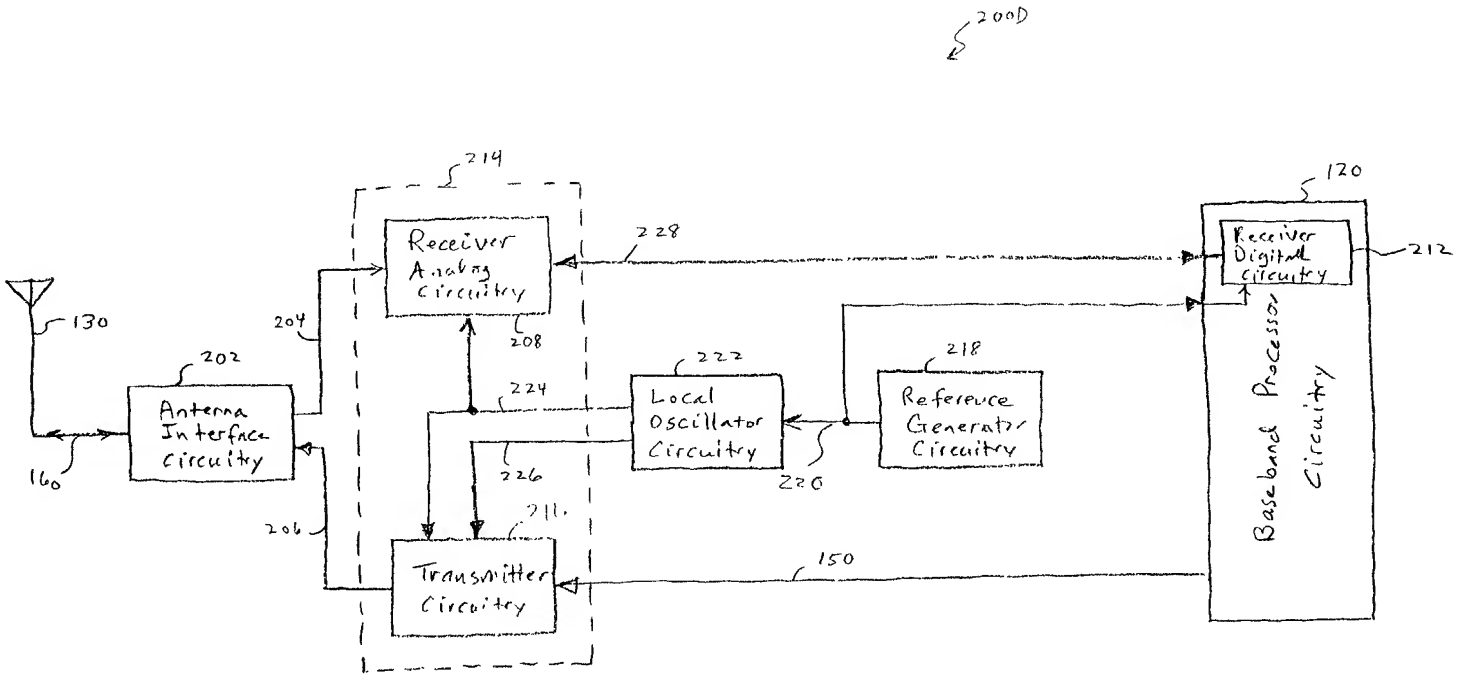

200D
214
Receiver Analog Circuitry
208
228
120
Receiver Digital Circuitry
212
Baseband Processor Circuitry
130
204
202
Antenna Interface Circuitry
160
224
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
226
206
211
Transmitter Circuitry
150

FIG. 2D

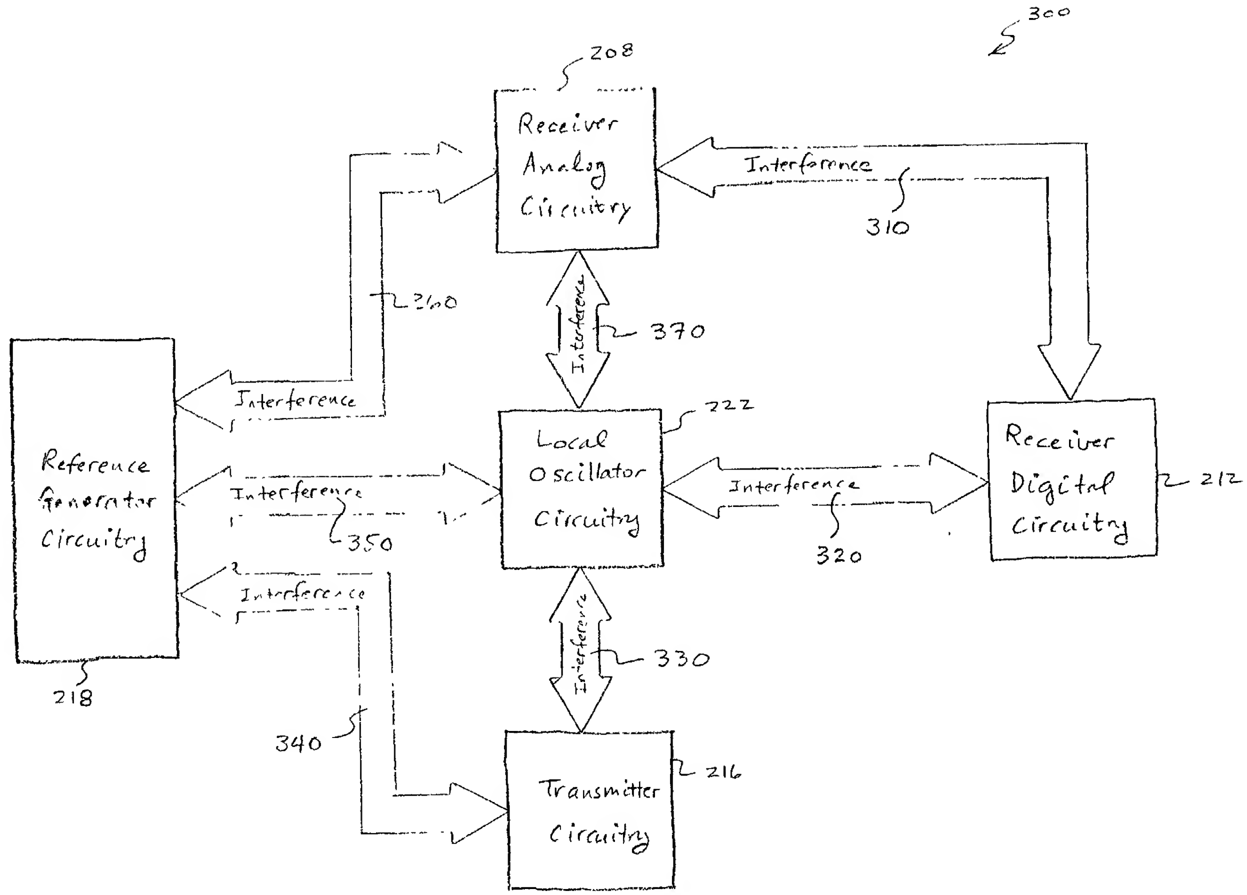

300
208
Receiver Analog Circuitry
Interference
310
360
370
Interference
Reference Generator Circuitry
218
Interference
222
Local Oscillator Circuitry
Interference
320
Receiver Digital Circuitry
212
Interference
350
Interference
330
Interference
340
Transmitter Circuitry
216

FIG. 3

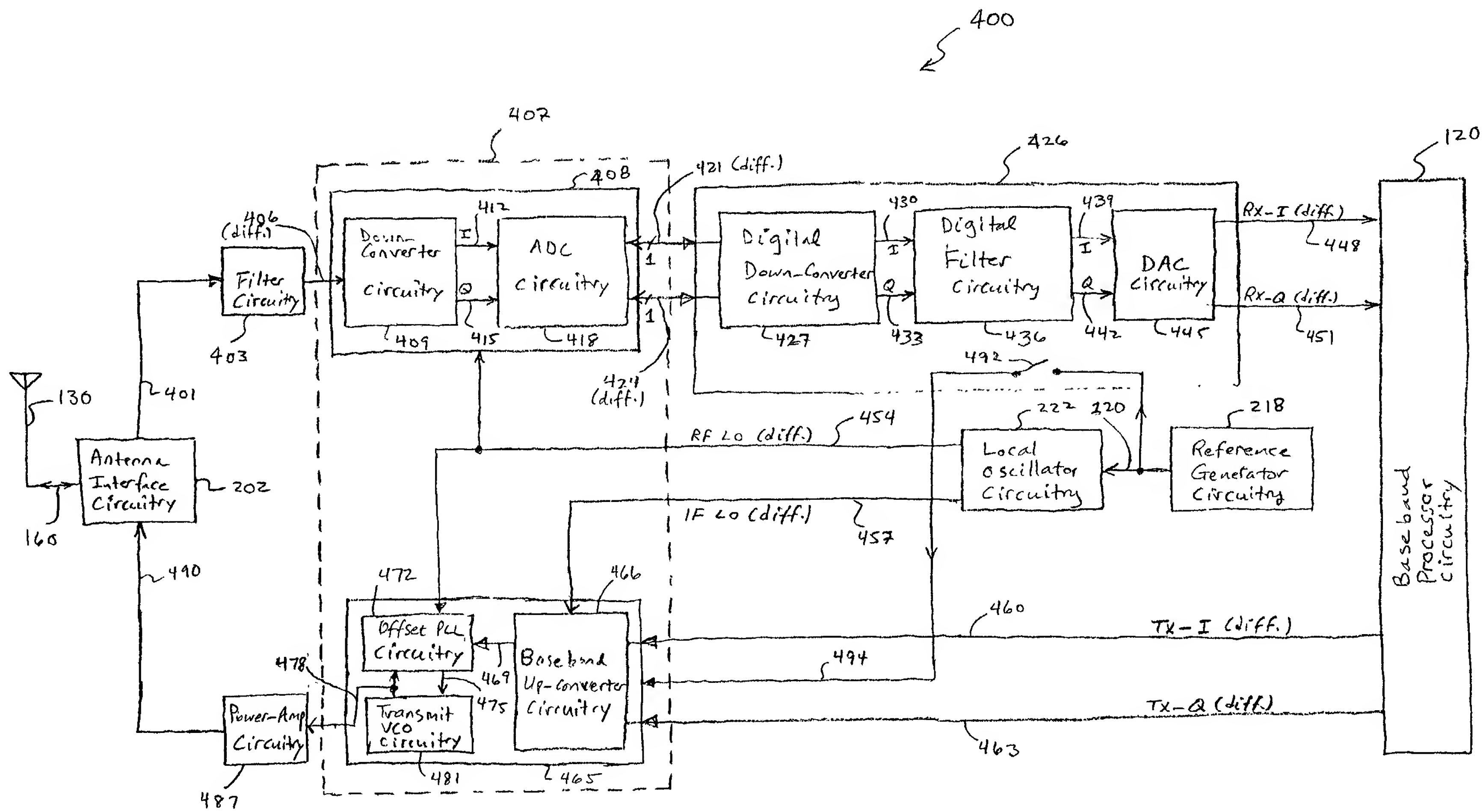

400
402
408
426
120
Down-Converter circuitry
409
ADC circuitry
418
412
415
I
Q
Filter Circuitry
403
406 (diff.)
421 (diff.)
424 (diff.)
1
1
Digital Down-Converter circuitry
427
430
433
Digital Filter Circuitry
436
439
442
DAC circuitry
445
Rx-I (diff.)
448
Rx-Q (diff.)
451
Baseband Processor circuitry
Antenna Interface Circuitry
202
130
160
401
490
RF LO (diff.)
454
IF LO (diff.)
457
492
222
220
Local Oscillator Circuitry
Reference Generator Circuitry
218
Offset PLL Circuitry
472
Baseband Up-Converter Circuitry
466
469
475
Transmit VCO circuitry
481
465
478
Power-Amp Circuitry
487
TX-I (diff.)
460
494
TX-Q (diff.)
463

FIG. 4

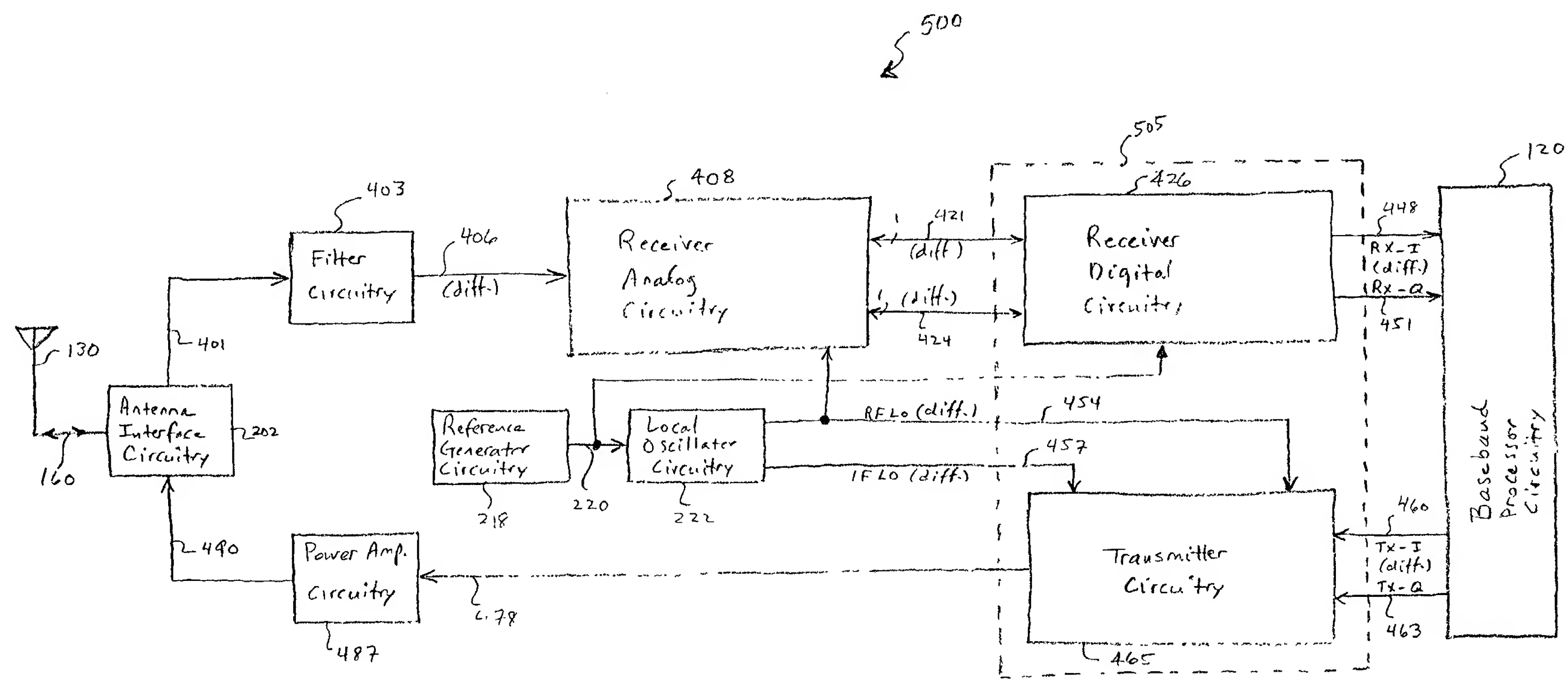

500
130
160
Antenna Interface Circuitry
202
401
403
Filter Circuitry
406
(diff.)
408
Receiver Analog Circuitry
421
(diff.)
(diff.)
424
505
426
Receiver Digital Circuitry
448
RX-I
(diff.)
RX-Q
451
120
Baseband Processor Circuitry
Reference Generator Circuitry
218
220
Local Oscillator Circuitry
222
RF LO (diff.)
454
IF LO (diff.)
457
Transmitter Circuitry
465
460
TX-I
(diff.)
TX-Q
463
Power Amp. Circuitry
487
490
478

FIG. 5

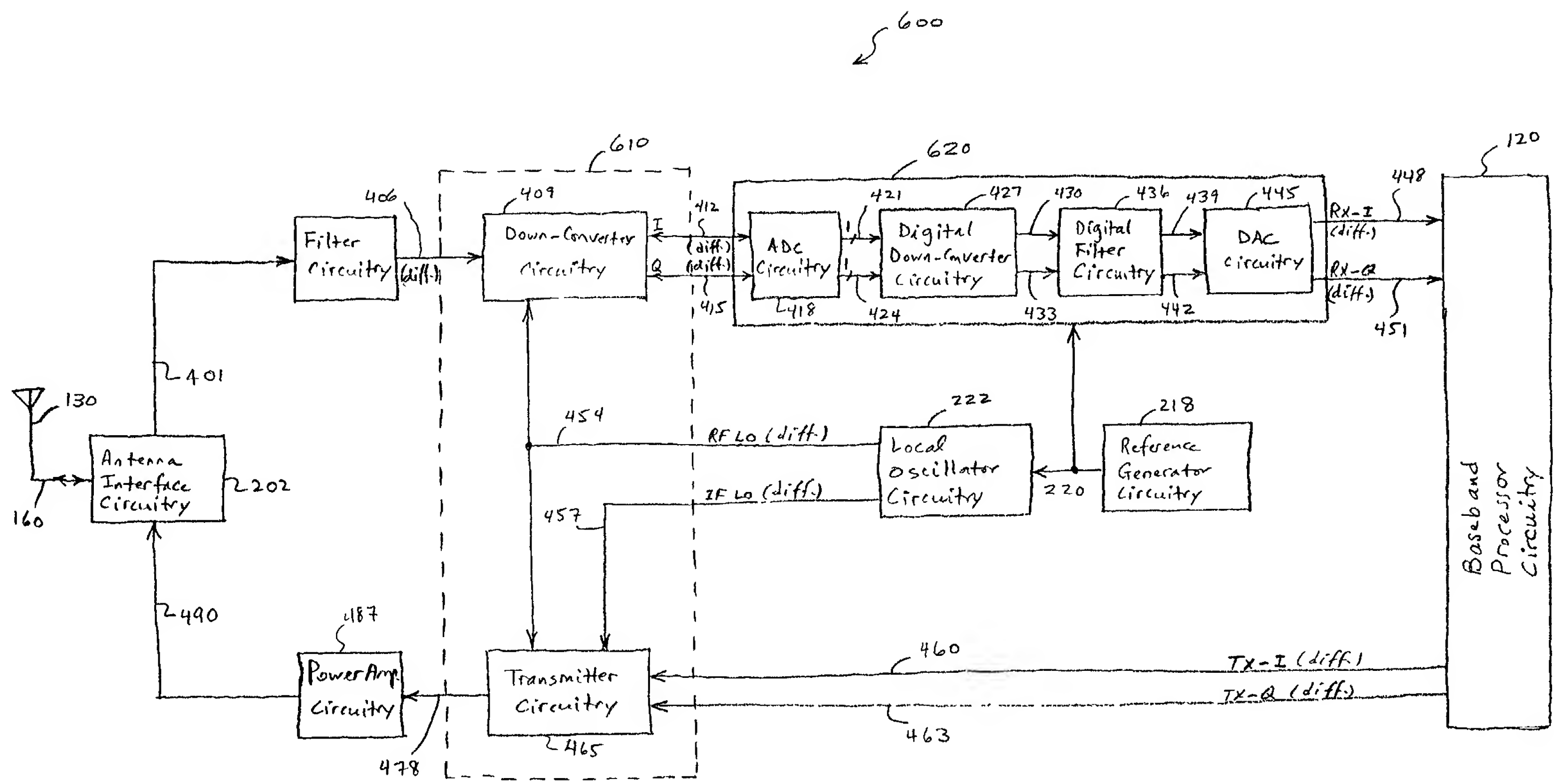

600
610
620
120
Antenna Interface Circuitry
130
160
202
401
490
Filter Circuitry
406
(diff.)
Down-Converter Circuitry
409
I
Q
412
(diff.)
(diff.)
415
ADC Circuitry
418
421
424
Digital Down-Converter Circuitry
427
430
433
Digital Filter Circuitry
436
439
442
DAC circuitry
445
RX-I
(diff.)
448
RX-Q
(diff.)
451
Baseband Processor Circuitry
Local Oscillator Circuitry
222
Reference Generator Circuitry
218
220
RF LO (diff.)
454
IF LO (diff.)
457
Transmitter Circuitry
465
TX-I (diff.)
460
TX-Q (diff.)
463
Power Amp Circuitry
487
478

FIG. 6

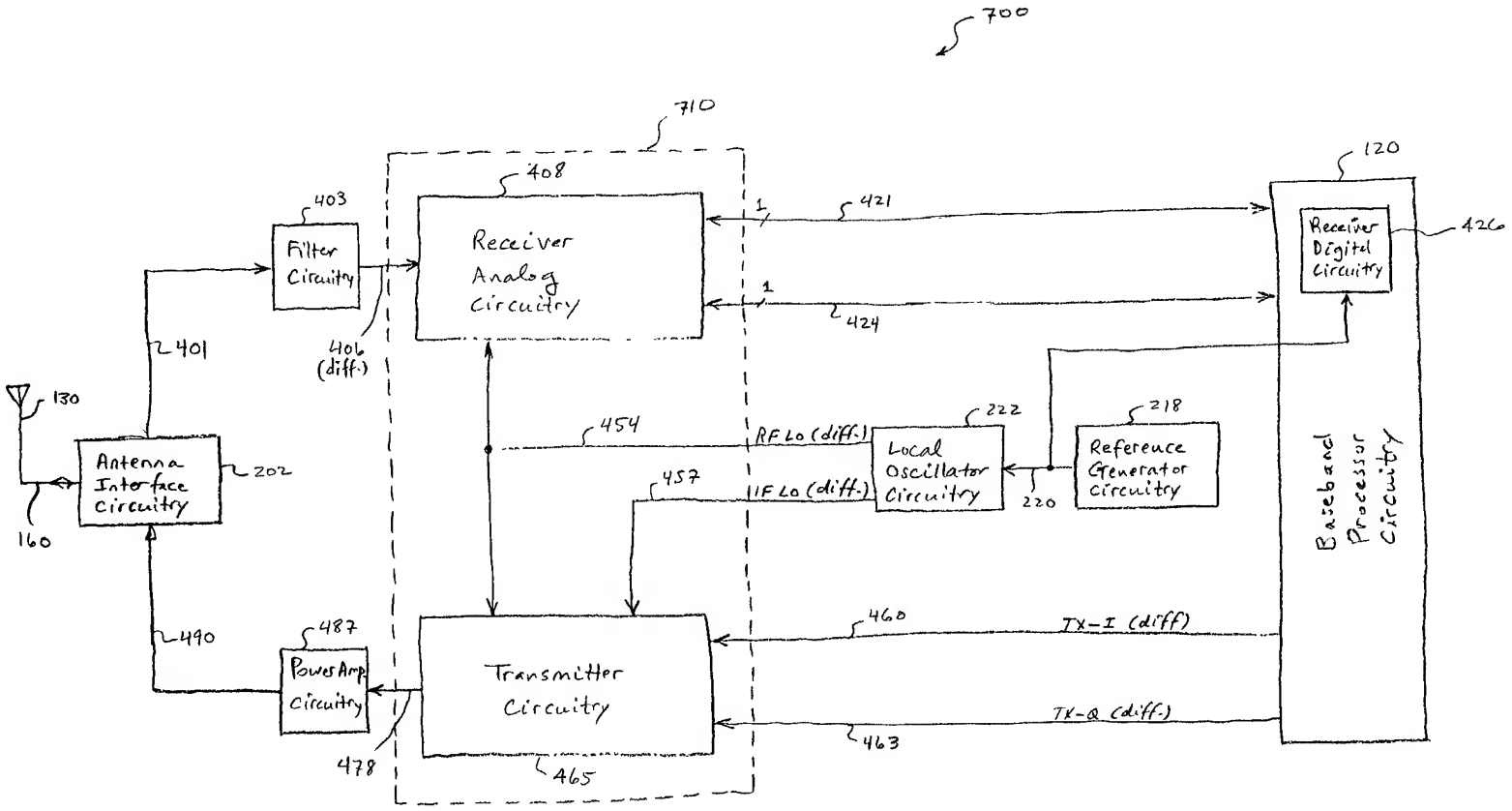
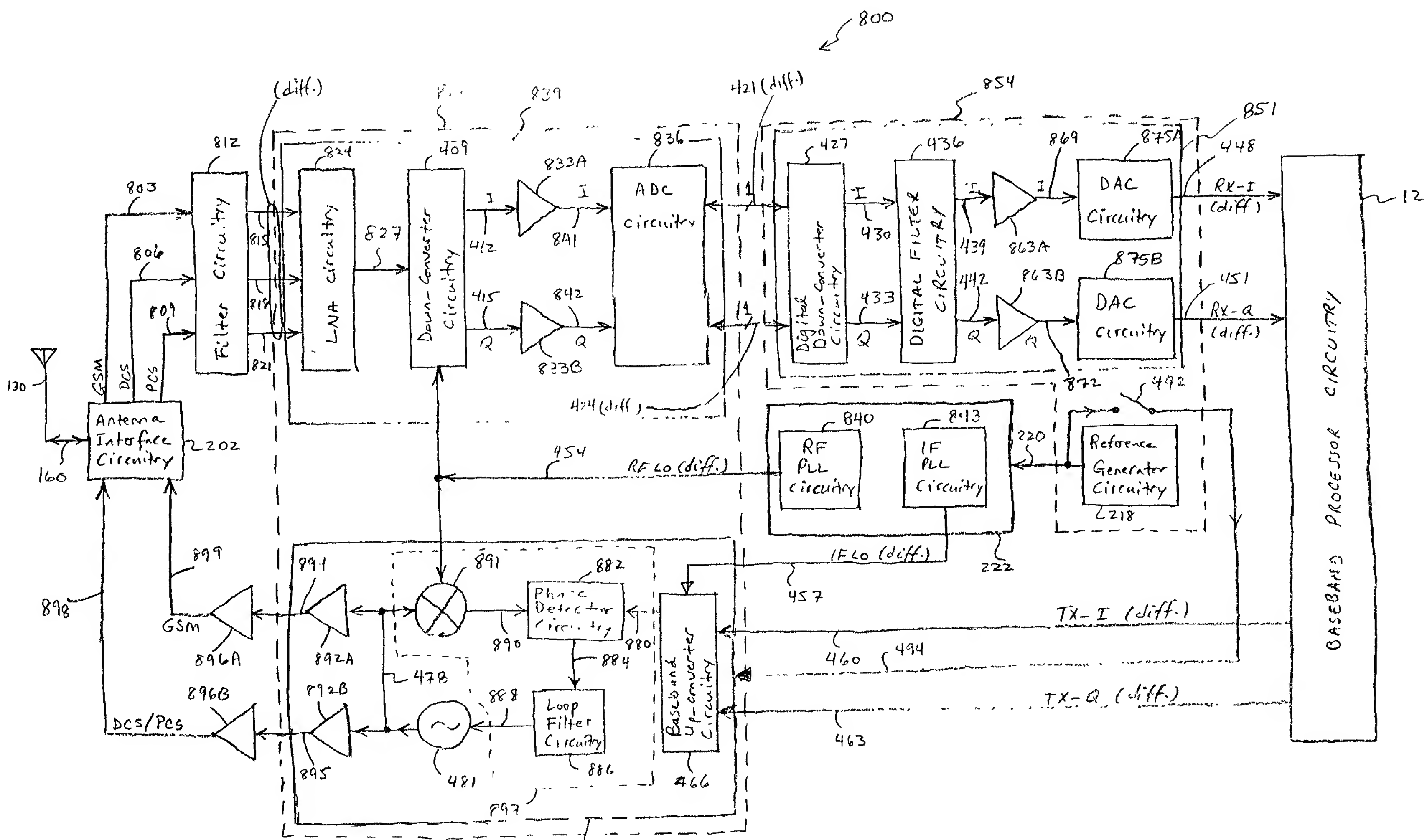

700
710
408
403
Filter Circuitry
Receiver Analog Circuitry
1
421
120
Receiver Digital Circuitry
426
1
424
406 (diff.)
401
130
Antenna Interface Circuitry
202
160
454
RF LO (diff.)
222
Local Oscillator Circuitry
218
Reference Generator circuitry
220
457
IF LO (diff.)
Baseband Processor Circuitry
460
TX-I (diff)
490
487
Power Amp Circuitry
Transmitter Circuitry
TX-Q (diff.)
463
478
465

FIG. 7



800
Antenna Interface Circuitry
Filter Circuitry
LNA circuitry
Down-Converter Circuitry
ADC circuitry
Digital Down-Converter Circuitry
DIGITAL FILTER CIRCUITRY
DAC Circuitry
DAC Circuitry
BASEBAND PROCESSOR CIRCUITRY
RF PLL circuitry
IF PLL Circuitry
Reference Generator Circuitry
Phase Detector Circuitry
Loop Filter Circuitry
Baseband Up-converter Circuitry
GSM
DCS
PCS
DCS/PCS
(diff.)
421 (diff.)
424 (diff.)
RF LO (diff.)
IF LO (diff.)
RX-I (diff.)
RX-Q (diff.)
TX-I (diff.)
TX-Q (diff.)
I
Q
120
130
160
202
218
220
222
409
412
415
427
430
433
436
439
442
448
451
454
457
460
463
466
478
481
492
494
803
806
809
812
815
818
821
824
827
833A
833B
836
839
840
841
842
851
854
863A
863B
869
872
875A
875B
877
880
882
884
886
888
890
891
892A
892B
894
895
896A
896B
897
898
899

FIG. 8

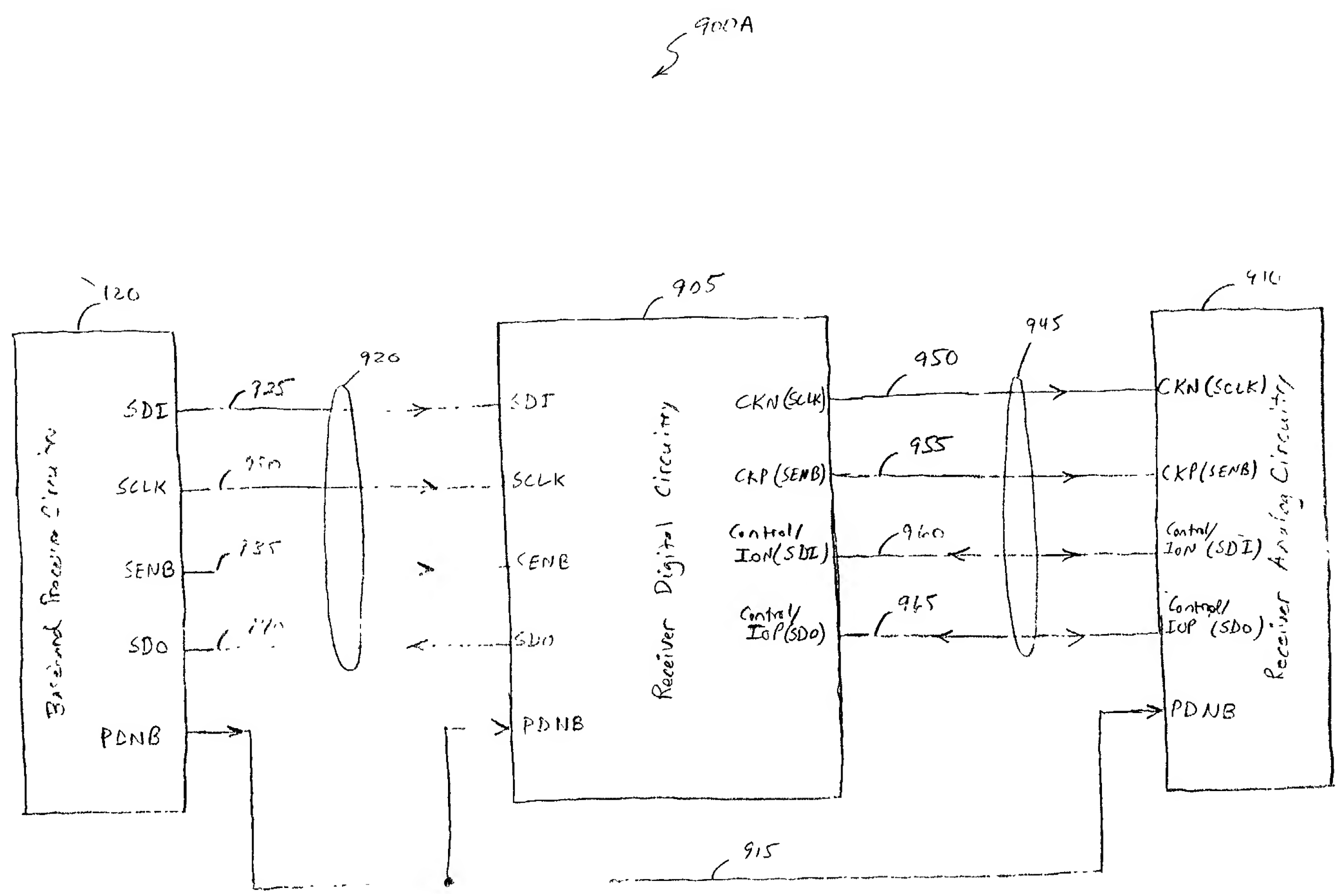

900A
120
Baseband Processor Circuit
SDI
SCLK
SENB
SDO
PDNB
725
735
920
905
Receiver Digital Circuitry
SDI
SCLK
SENB
SDO
PDNB
CKN(SCLK)
CKP(SENB)
Control/ ION(SDI)
Control/ IOP(SDO)
950
955
960
965
945
910
Receiver Analog Circuitry
CKN(SCLK)
CKP(SENB)
Control/ ION (SDI)
Control/ IOP (SDO)
PDNB
915

FIG. 9A

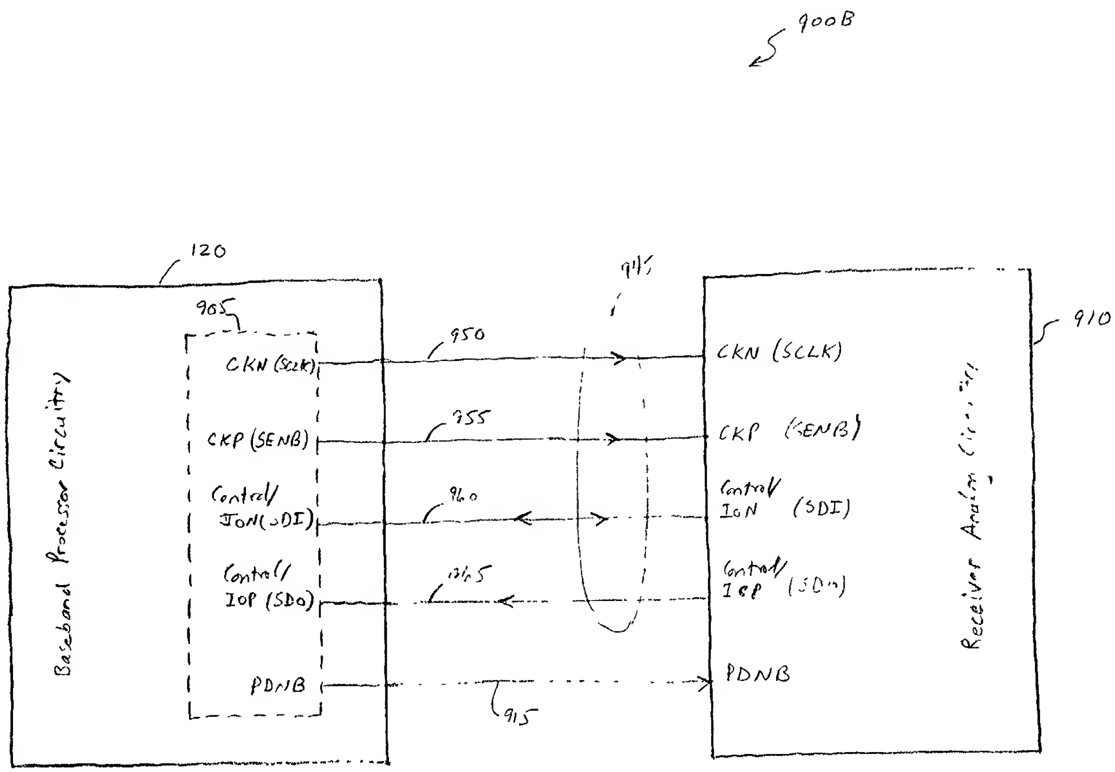

900B
120
905
Baseband Processor Circuitry
CKN (SCLK)
CKP (SENB)
Control/
ION (SDI)
Control/
IOP (SDO)
PDNB
950
955
960
915
910
CKN (SCLK)
CKP (SENB)
Control/
ION (SDI)
Control/
PDNB

FIG. 9B

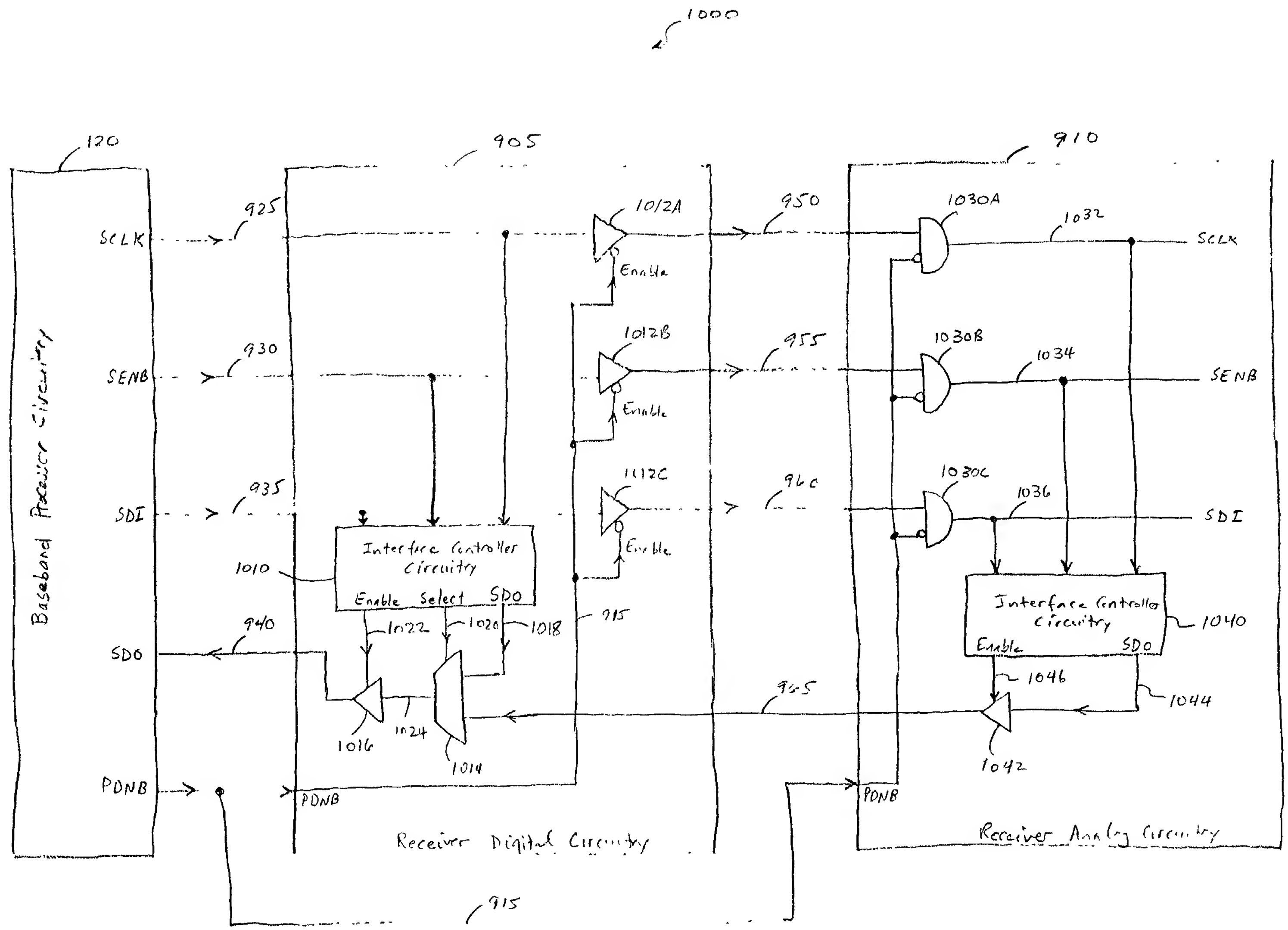

1000
120
Baseband Processor Circuitry
SCLK
SENB
SDI
SDO
PDNB
925
930
935
940
905
Receiver Digital Circuitry
Interface Controller Circuitry
Enable
Select
SDO
1010
1012A
1012B
1112C
Enable
1014
1016
1018
1020
1022
1024
915
950
955
960
965
910
Receiver Analog Circuitry
1030A
1030B
1030C
1032
1034
1036
Interface Controller Circuitry
1040
1042
1044
1046

FIG. 10

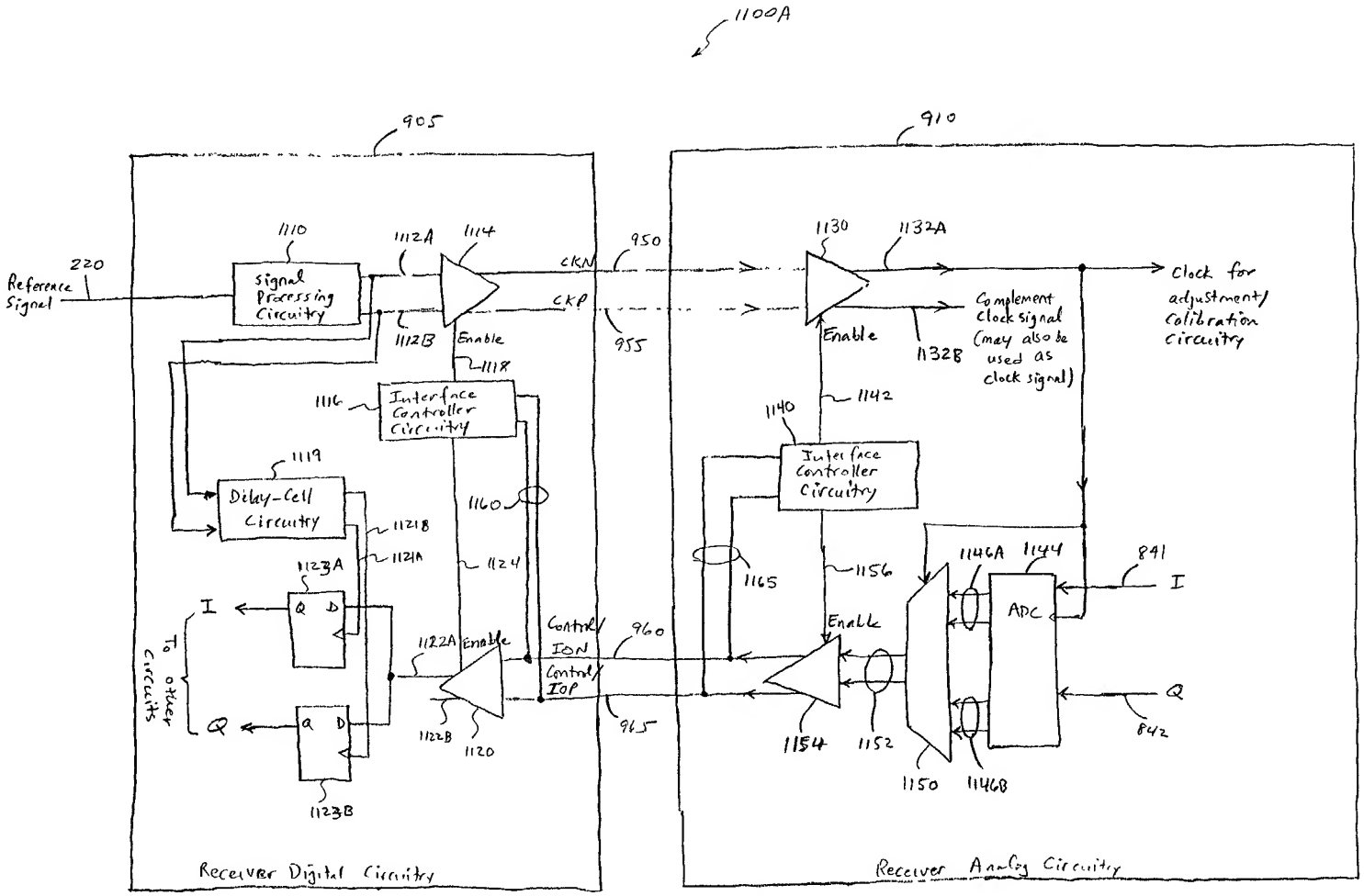

1100A
905
910
220
Reference Signal
1110
Signal Processing Circuitry
1112A
1114
1112B
Enable
1118
1116
Interface Controller Circuitry
1119
Delay-Cell Circuitry
1121B
1121A
1123A
1123B
1124
1160
I
Q
To other circuits
1122A
1122B
1120
Enable
Control ION
Control IOP
960
965
950
955
CKN
CKP
1130
1132A
1132B
Enable
Complement clock signal (may also be used as clock signal)
Clock for adjustment/ calibration circuitry
1140
Interface Controller Circuitry
1142
1165
1156
1146A
1144
841
I
ADC
Q
842
Enable
1154
1152
1150
1146B
Receiver Digital Circuitry
Receiver Analog Circuitry

FIG. 11A

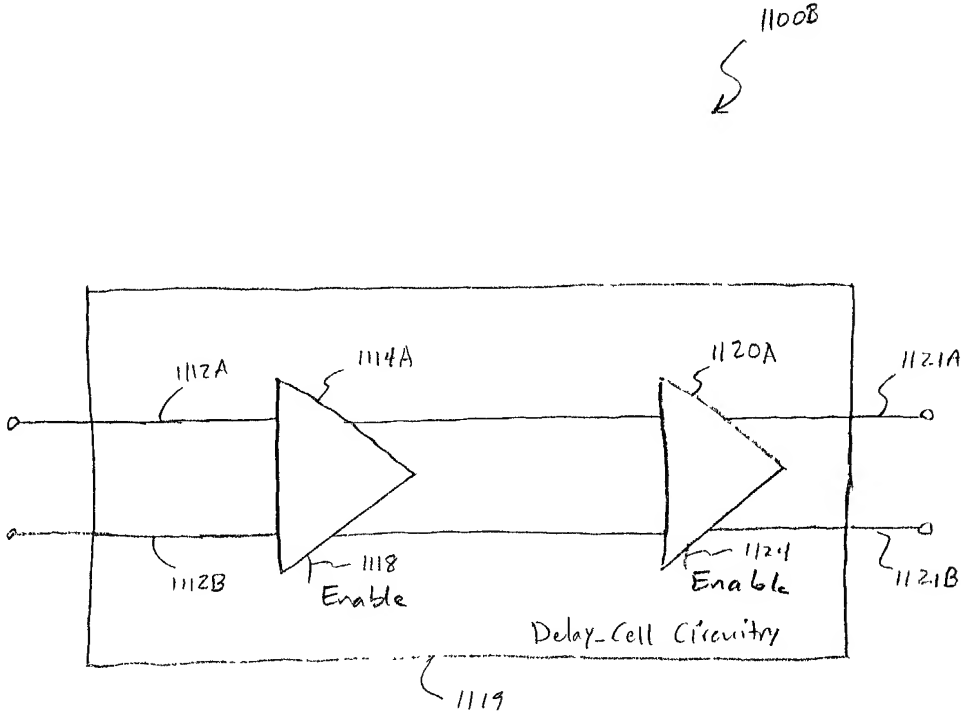


FIG. 11B

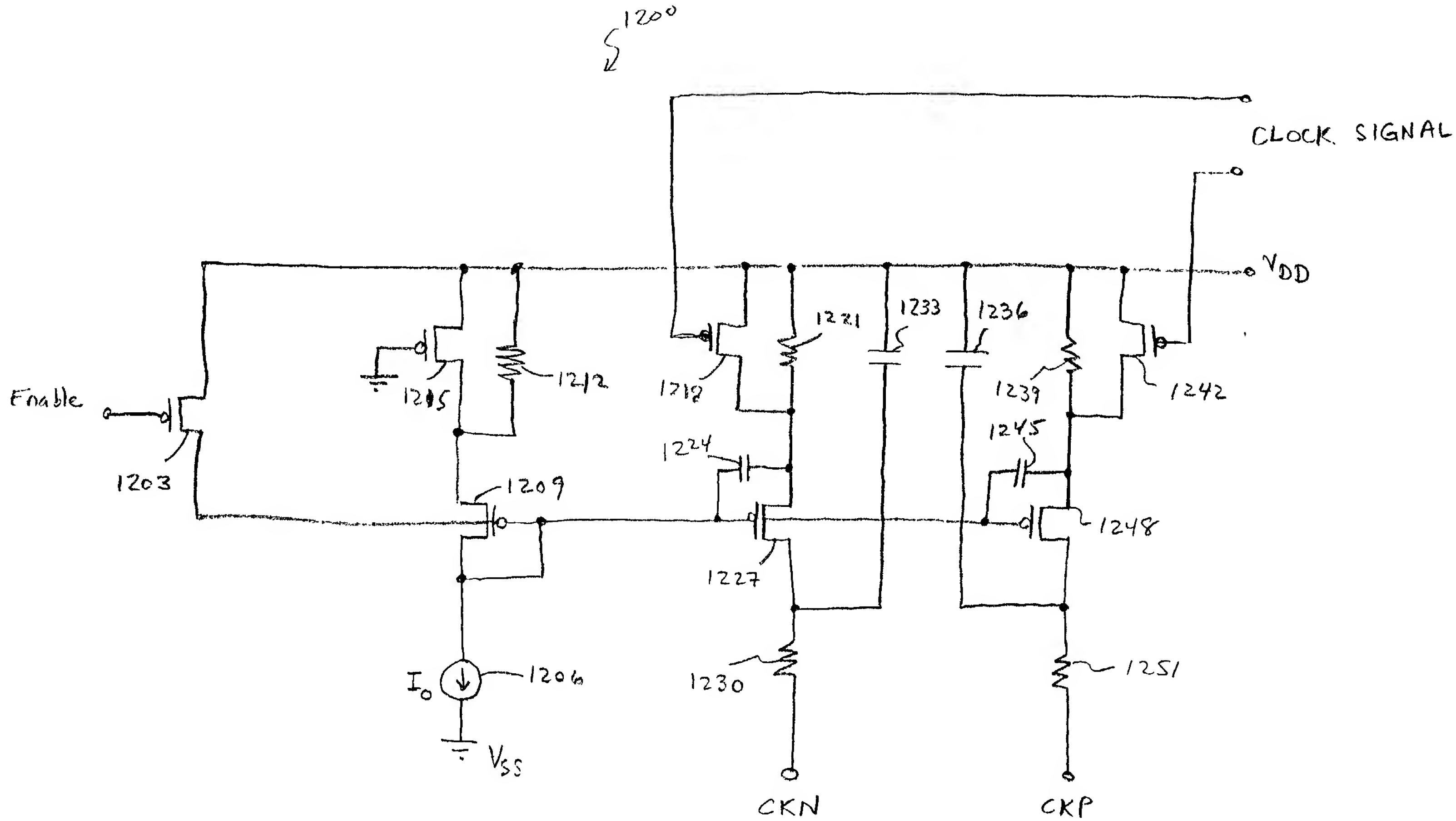

1200
CLOCK SIGNAL
VDD
Enable
1203
1215
1212
1209
1206
I_o
V_{SS}
1218
1221
1224
1227
1230
1233
1236
1239
1242
1245
1248
1251
CKN
CKP

FIG. 12

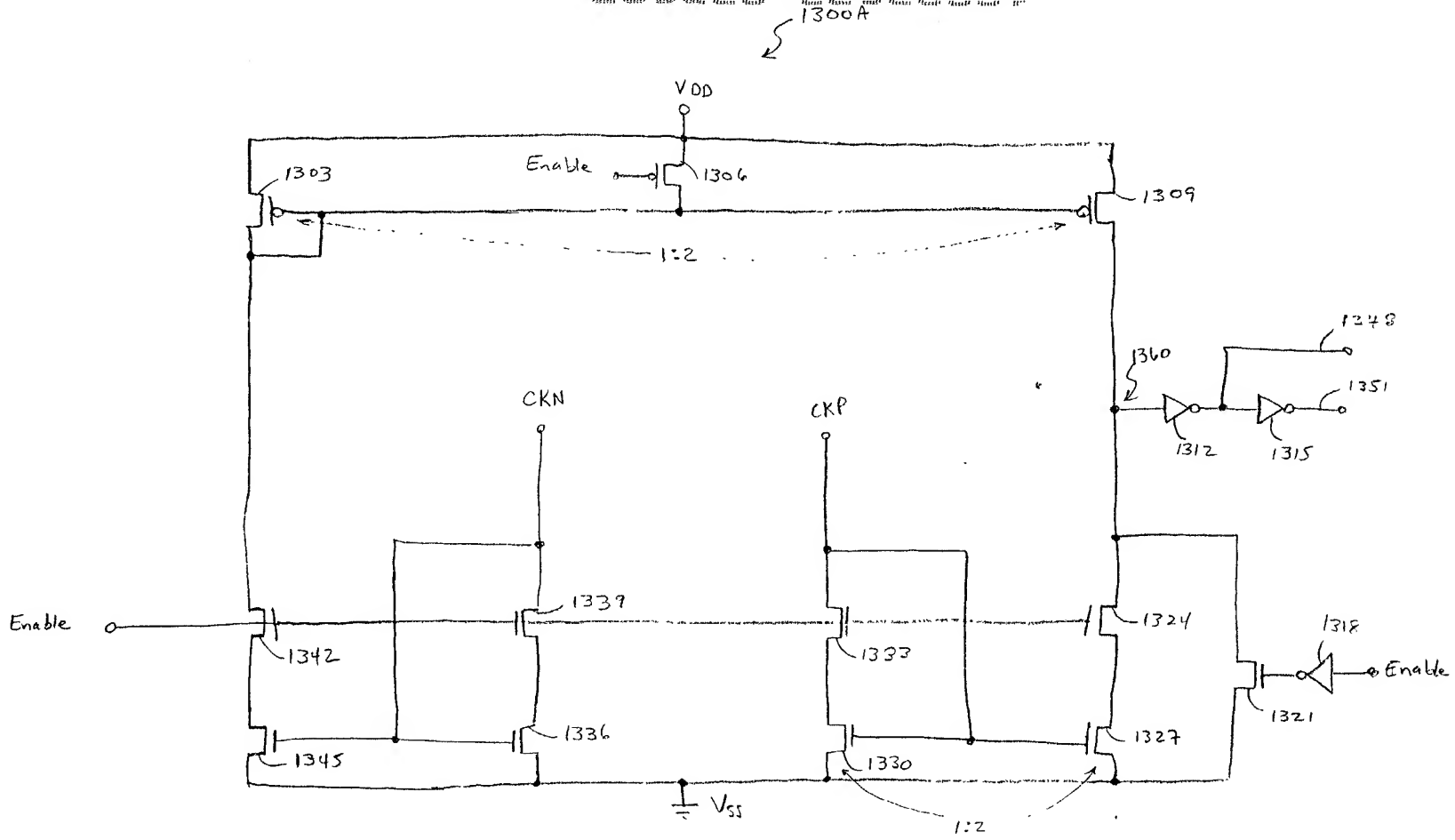

1300A
VDD
Enable
1306
1303
1309
1:2
1348
1360
1351
CKN
CKP
1312
1315
Enable
1339
1342
1333
1324
1318
Enable
1321
1336
1345
1327
1330
Vss
1:2

FIG. 13A

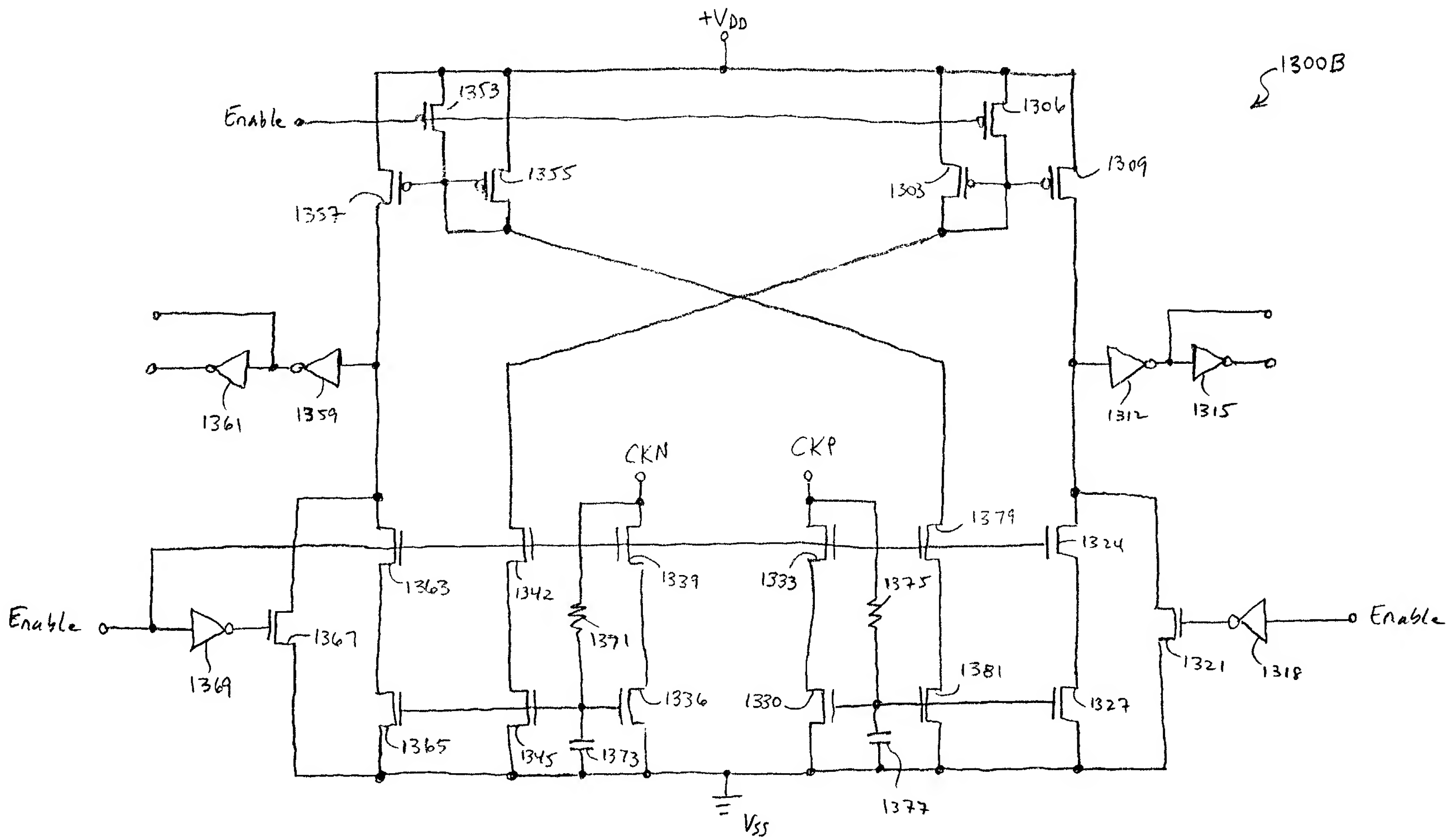

+VDD
1300B
Enable
1353
1355
1357
1306
1303
1309
1361
1359
1312
1315
CKN
CKP
1379
1324
1363
1342
1339
1333
1375
Enable
1367
1369
1371
1321
1318
Enable
1381
1336
1330
1327
1365
1345
1373
1377
Vss

FIG. 13B

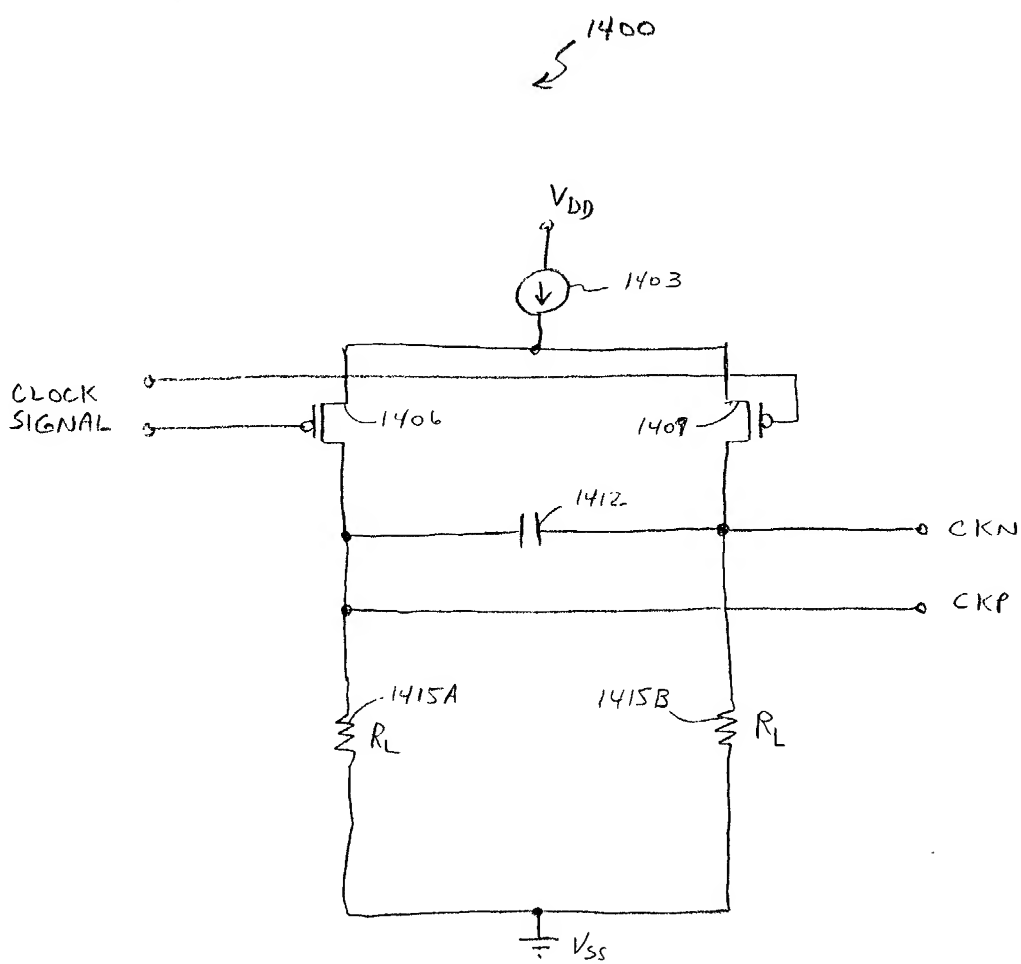

1400
V_{DD}
1403
CLOCK
SIGNAL
1406
1409
1412
CKN
CKP
1415A
R_L
1415B
R_L
V_{SS}

FIG. 14

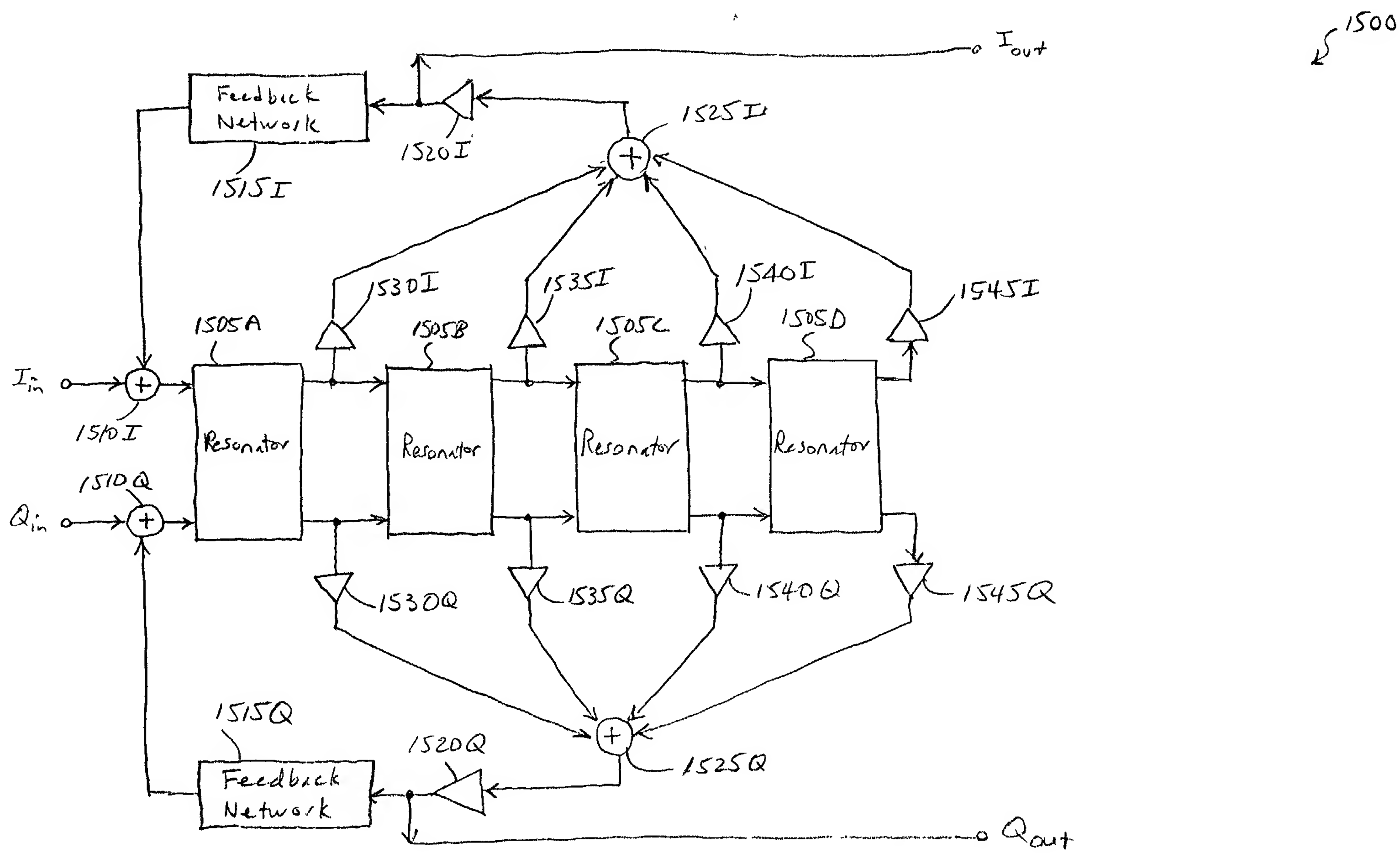

1500
I_{out}
Feedback Network
1515I
1520I
1525I
1530I
1535I
1540I
1545I
1505A
1505B
1505C
1505D
I_{in}
1510I
Resonator
Resonator
Resonator
Resonator
1510Q
Q_{in}
1530Q
1535Q
1540Q
1545Q
1515Q
1520Q
1525Q
Feedback Network
Q_{out}

FIG. 15

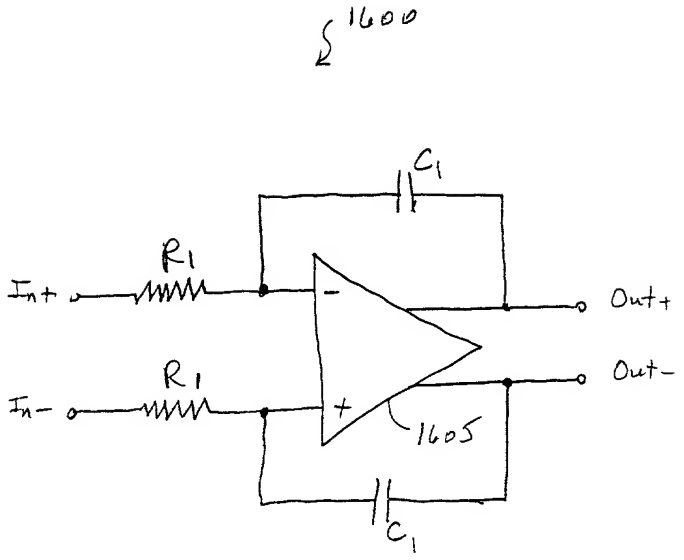

1600
C1
R1
In+
R1
In-
Out+
Out-
1605
C1

FIG. 16

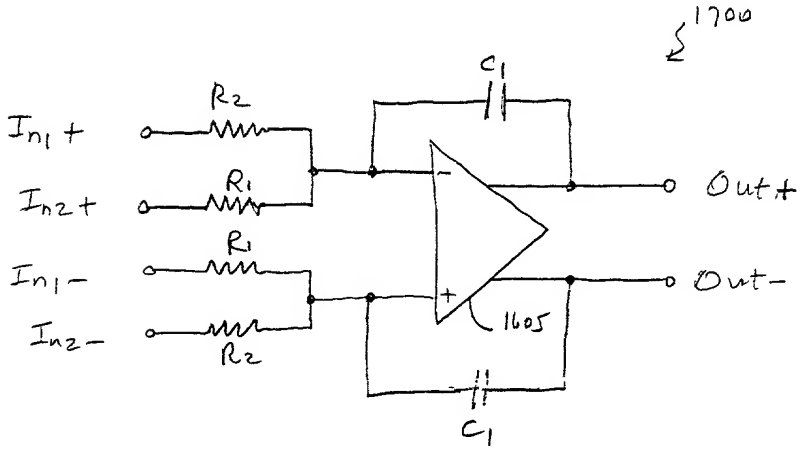

1700
C1
R2
In1+
R1
In2+
R1
In1-
In2-
R2
Out+
Out-
1605
C1

FIG. 17

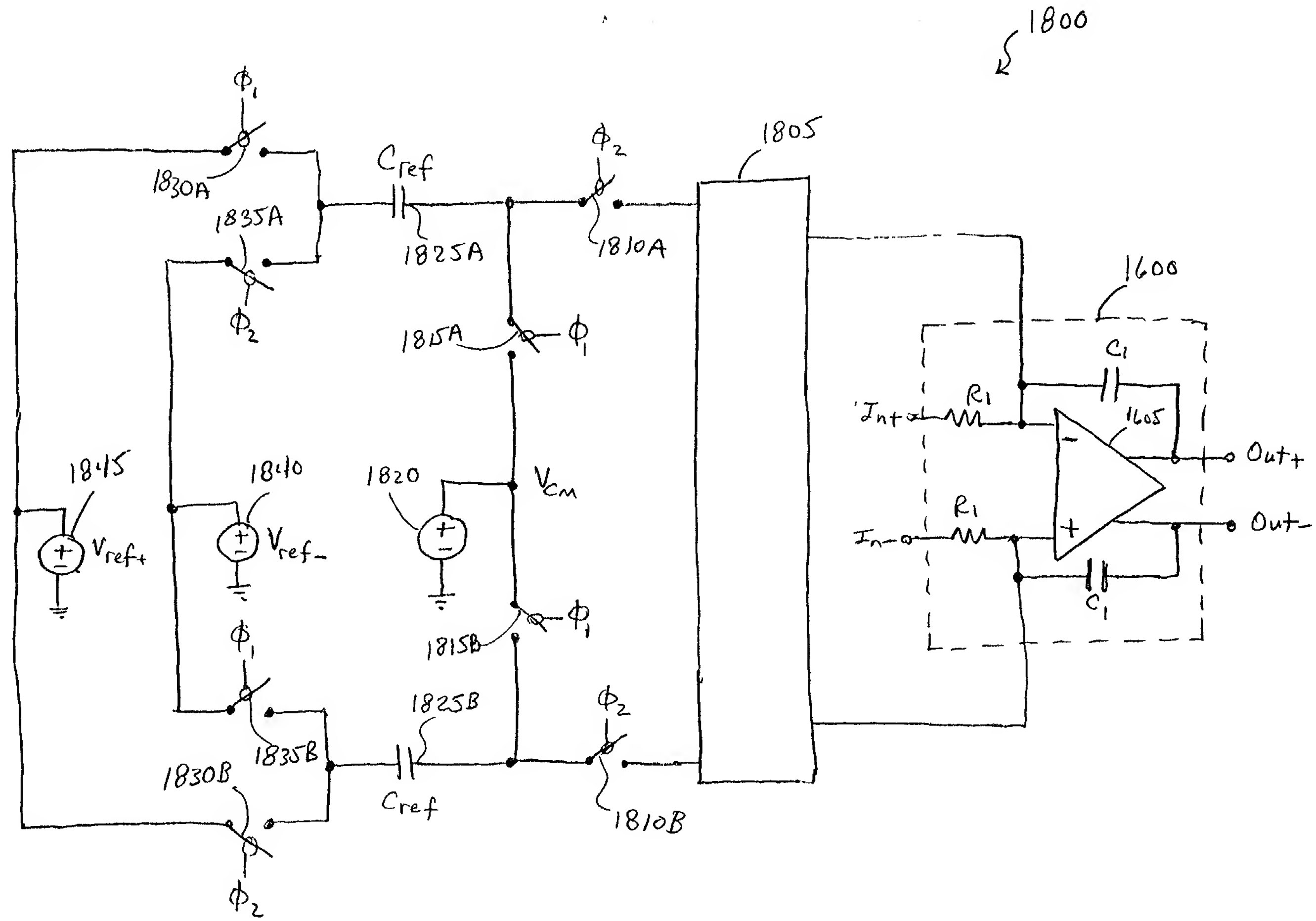

1800
1805
1600
1605
C_1
C_1
R_1
R_1
In_+
In_-
Out_+
Out_-
Φ_1
Φ_2
Φ_2
Φ_1
Φ_1
Φ_1
Φ_2
Φ_2
1830A
1835A
1825A
1810A
1815A
C_{ref}
1845
V_{ref+}
1840
V_{ref-}
1820
V_{CM}
1815B
1835B
1830B
1825B
C_{ref}
1810B

FIG. 18

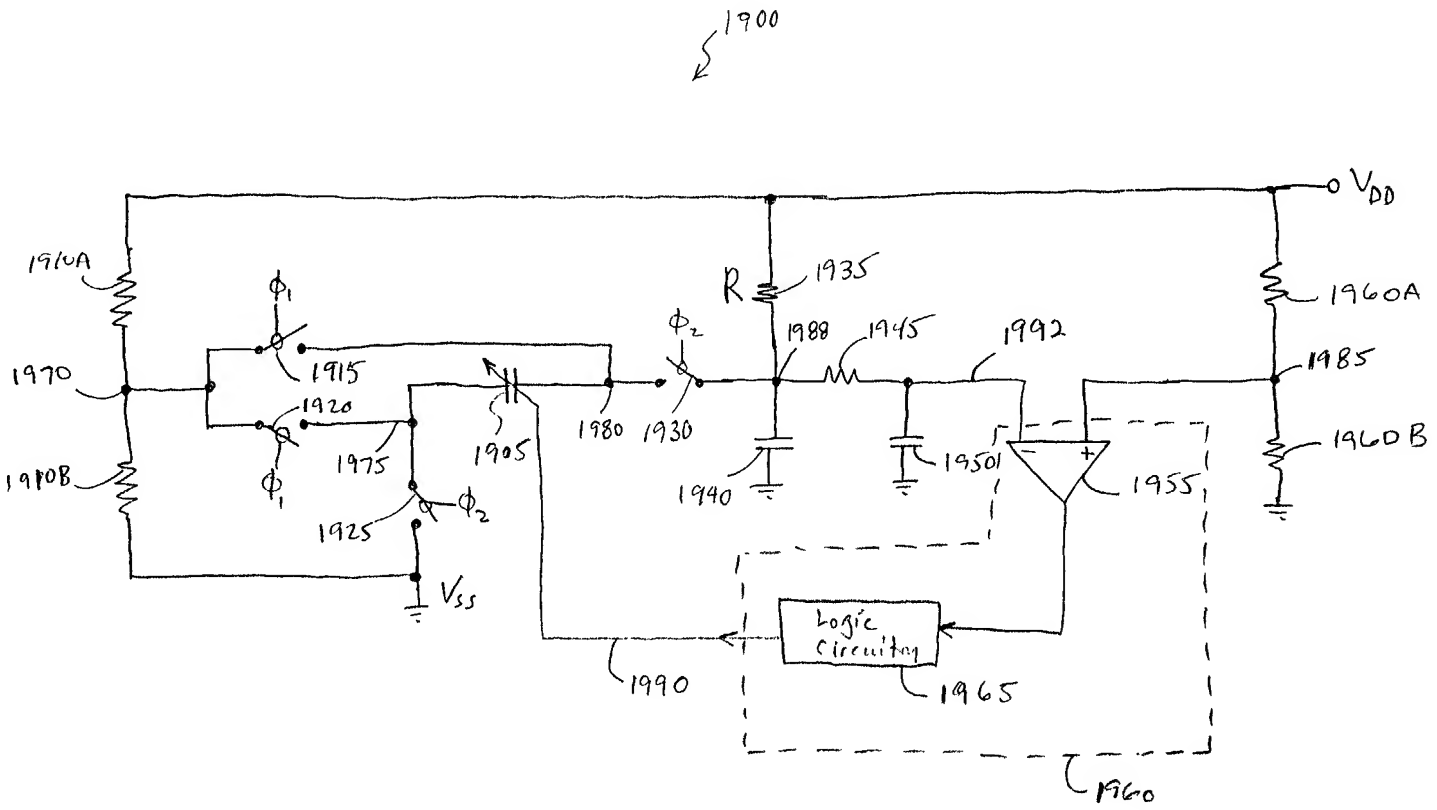


FIG. 19

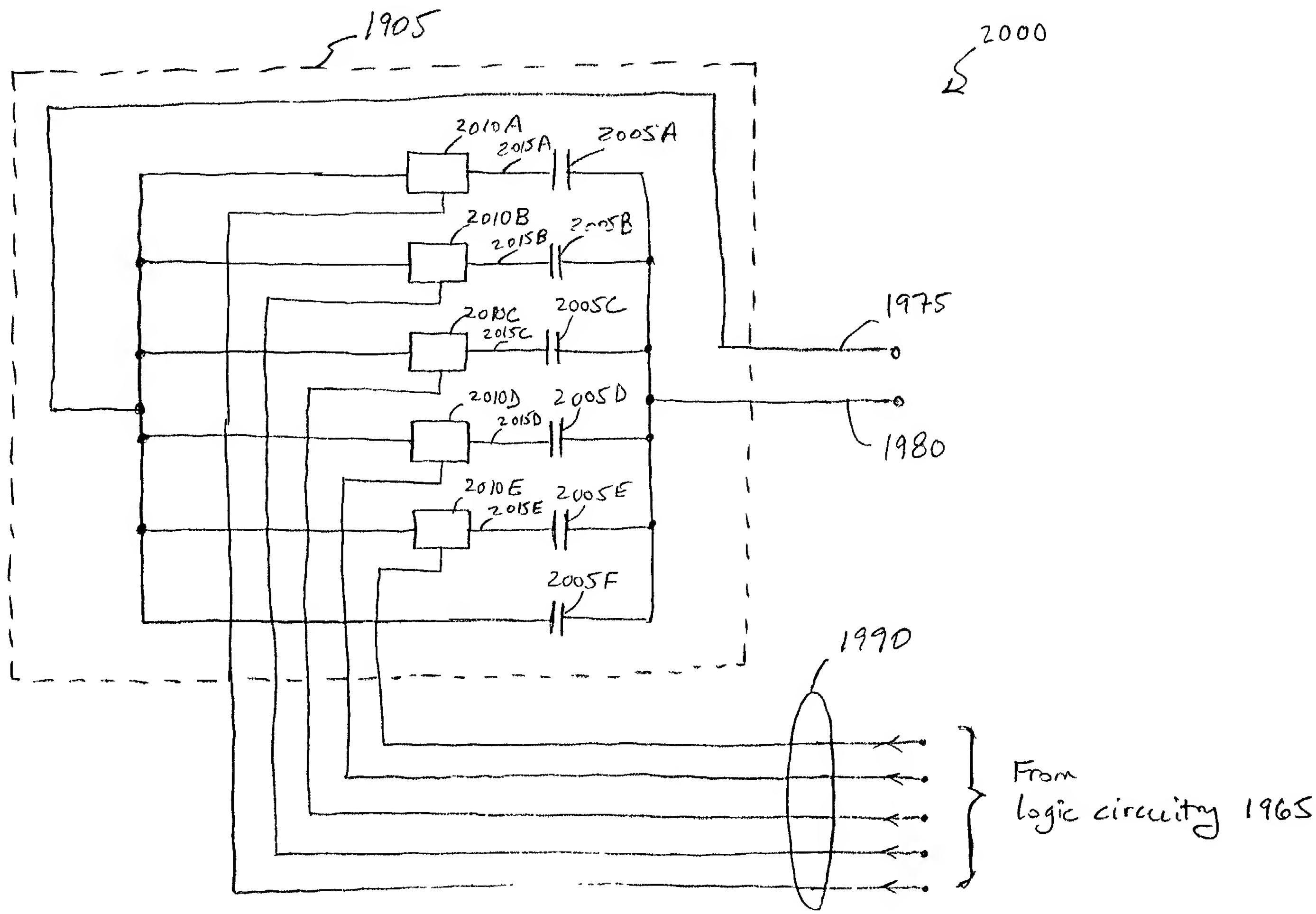

1905
2000
2010A
2015A
2005A
2010B
2015B
2005B
2010C
2015C
2005C
2010D
2015D
2005D
2010E
2015E
2005E
2005F
1975
1980
1990
From
logic circuitry 1965

FIG. 20

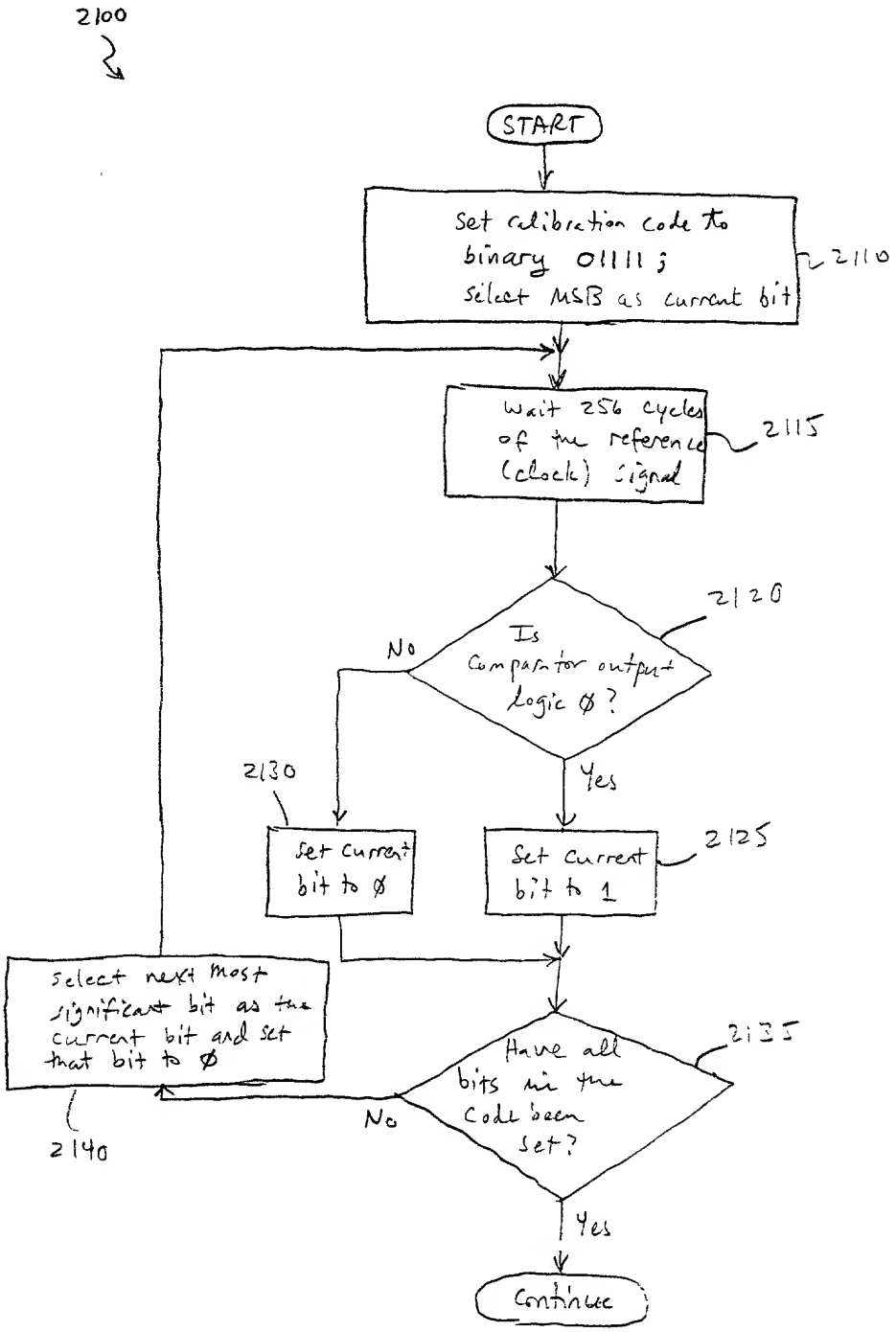

2100
START
Set calibration code to binary 01111; select MSB as current bit
2110
Wait 256 cycles of the reference (clock) signal
2115
2120
Is Comparator output logic Ø?
No
Yes
2130
Set current bit to Ø
Set current bit to 1
2125
Select next most significant bit as the current bit and set that bit to Ø
2140
2135
Have all bits in the code been set?
No
Yes
Continue

FIG. 21